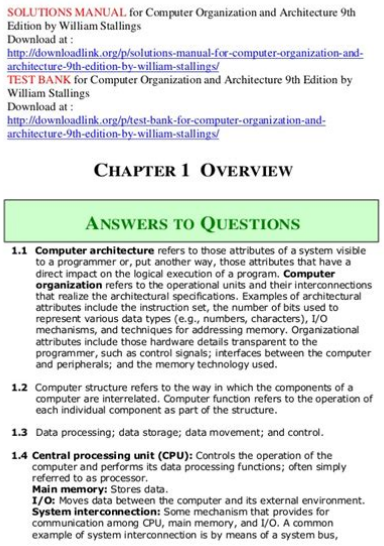

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CHAPTER 1 OVERVIEW

ANSWERS TO QUESTIONS

1.1 **Computer architecture** refers to those attributes of a system visible to a programmer or, put another way, those attributes that have a direct impact on the logical execution of a program. **Computer organization** refers to the operational units and their interconnections that realize the architectural specifications. Examples of architectural attributes include the instruction set, the number of bits used to represent various data types (e.g., numbers, characters), I/O mechanisms, and techniques for addressing memory. Organizational attributes include those hardware details transparent to the programmer, such as control signals; interfaces between the computer and peripherals; and the memory technology used.

1.2 Computer structure refers to the way in which the components of a computer are interrelated. Computer function refers to the operation of each individual component as part of the structure.

1.3 Data processing; data storage; data movement; and control.

1.4 **Central processing unit (CPU):** Controls the operation of the computer and performs its data processing functions; often simply referred to as processor.
Main memory: Stores data.
I/O: Moves data between the computer and its external environment.
System interconnection: Some mechanism that provides for communication among CPU, main memory, and I/O. A common example of system interconnection is by means of a system bus,

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Interface control pins\n\nControl the timing of transactions and provide coordination among initiators and\n\ntargets. Arbitration pins Unlike the other PCI signal lines, these are not shared\n\nlines. Rather, each PCI master has its own pair of arbitration lines that connect

it\n\ndirectly to the PCI bus arbiter. Error Reporting pins Used to report parity and\n14\n\n \n\f3.1\n\n3.2\n\n3.3\n\nother errors. Interrupt Pins These are provided for PCI devices that must generate\nrequests for service. The value in the MBR is loaded int\n6. a\n\nb. The value in the AC is loaded into\n\nc. However, because the data bus is only 16 bits, it\nwill require 2 cycles to fetch a 32bit instruction or operand.\n\n2 The 16 bits of the address placed on the address bus cant access the whole\nmemory. Thus a more complex memory interface control is needed to latch the\nfirst part of the address and then the second part because the microprocessor\nwill end in two steps. The CPU, which is much faster\nhan the Teletype, must repeatedly check FGI and FGO. If interrupts are used,\nhe Teletype can issue an interrupt to the CPU whenever it is ready to accept or\nsend data. The IEN register can be set by the CPU under programmer control\n\na. During a single bus cycle, the 8bit microprocessor transfers one byte while the\n6bit microprocessor transfers two bytes. The 16bit microprocessor has twice\nhe data transfer rate.\n\nb. Suppose we do 100 transfers of operands and instructions, of which 50 are one\nbyte long and 50 are two bytes long. Thus, the data transfer rates differ by a factor of 1.5.\n\nThe whole point of the clock is to define event times on the bus; therefore, we wish\nfor a bus arbitration operation to be made each clock cycle. This requires that the\npriority signal propagate the length of the daisy chain Figure 3.26 in one clock\nperiod.http://xn----7sbab1bcaqplb0ccyi9d.xn--p1ai/files/87-trx250x-manual.xml

Thus, the maximum number of masters is determined by dividing the\namount of time it takes a bus master to pass through the bus priority by the clock\nperiod.\n\nThe lowestpriority device is assigned priority 16. This device must defer to all the\nothers. However, it may transmit in any slot not reserved by the other SBI devices.\n\nAt the beginning of any slot, if none of the TR lines is asserted, only the priority 16\ndevice may transmit. This gives it the lowest average wait time under most\ncircumstances. The\nlength of the memory read cycle is 300 ns.\n\nb. The Read signal begins to fall at 75 ns from the beginning of the third clock\ncycle middle of the second half of T,. Thus, memory must place the data on\n\nthe bus no later than 55 ns from the beginning of T,.\n\nThe clock period is 125 ns. Therefore, two clock cycles need to be inserted.\nFrom Figure 3.19, the Read signal begins to rise early in T. To insert two clock\n\ncycles, the Ready line can be put in low at the beginning of T, and kept low for\n250 ns.\n\noP\n\na. A5 MHz clock corresponds to a clock period of 200 ns. The\ninstruction requires four memory accesses, resulting in 8 wait states. The\ninstruction, with wait states, takes 24 clock cycles, for an increase of 50%.\n\nb. In this case, the instruction takes 26 bus cycles without wait states and 34 bus\ncycles with wait states, for an increase of 33%.\n\na. The clock period is 125 ns. If both operands are even\n\naligned, it takes 2 us to fetch the two operands. If one is oddaligned, the time\nrequired is 3 us. If both are oddaligned, the time required is 4 us.\n\n17\n\f3.17 Consider a mix of 100 instructions and operands. On average, they consist of 20 32\nbit items, 40 16bit items, and 40 bytes. For the 32bit microprocessor, the\nnumber required is 100. Access\nmust be made in a specific linear sequence. Direct access Individual blocks or\nrecords have a unique address based on physical location.

Access is accomplished\nby direct access to reach a general vicinity plus sequential searching, counting, or\nwaiting to reach the final location. Random access Each addressable location in\nmemory has a unique, physically wiredin addressing mechanism. The time to\naccess a given location is independent of the sequence of prior accesses and is\nconstant.\n\n \n\nFaster access time, greater cost per bit; greater capacity, smaller cost per bit; greater\ncapacity, slower access time.\n\nItis possible to organize data across a memory hierarchy such that the percentage\nof accesses to each successively lower level is substantially less than that of the\nlevel above. Because memory references tend to cluster, the data in the higher\nlevel memory need not change very often to satisfy memory access requests.\n\nIna cache system, direct mapping maps each block of main memory into only one\npossible cache line. Associative mapping permits each main memory block to be\nloaded into any line of the cache. In setassociative mapping, the cache is divided\ninto a number of sets of cache lines; each main memory block can be mapped into\nany line in a particular

set.\n\nOne field identifies a unique word or byte within a block of main memory. The\nremaining two fields specify one of the blocks of main memory. These two fields\nare a line field, which identifies one of the lines of the cache, and a tag field, which\nidentifies one of the blocks that can fit into that line.\n\nA tag field uniquely identifies a block of main memory. A word field identifies a\nunique word or byte within a block of main memory.\n\nOne field identifies a unique word or byte within a block of main memory. The\nremaining two fields specify one of the blocks of main memory. These two fields\nare a set field, which identifies one of the sets of the cache, and a tag field, which\nidentifies one of the blocks that can fit into that set.

\n\nSpatial locality refers to the tendency of execution to involve a number of memory\n\nlocations that are clustered. Temporal locality refers to the tendency fora\nprocessor to access memory locations that have been used recently.\n\n19\n\n \n\f4.9\n\n41\n\n4.2\n\n43\n\nSpatial locality is generally exploited by using larger cache blocks and by\nincorporating prefetching mechanisms fetching items of anticipated use into the\ncache control logic. Temporal locality is exploited by keeping recently used\ninstruction and data values in cache memory and by exploiting a cache hierarchy.\n\nA\ N \u00a9 PROBI\n\n \n\nThe cache is divided into 16 sets of 4 lines each. Therefore, 4 bits are needed to\nidentify the set number. Therefore, the\nset plus tag lengths must be 12 bits and therefore the tag length is 8 bits. Each\nblock contains 128 words. Thus the cache\nconsists of 256 sets of 2 lines each. Therefore 8 bits are needed to identify the set\nnumber. For the 64Mbyte main memory, a 26bit address is needed.Each set in the cache includes 3 LRU bits and four lines. The tag is used to distinguish between them.\n\n22\n\f4.9 a. The bits are set according to the following rules with each access to the set\n\n1. Solution Manual Computer Organization And Architecture 8th Edition.pdfMashhoods Web FamilyComputer Evolution and Performance. Computer Function and Interconnection. Cache Memory. Internal Memory. External Memory. Operating System Support. Computer Arithmetic.Instruction Sets Addressing Modes and Formats 80. Processor Structure and Function. 85. Reduced Instruction Set Computers 92. InstructionLevel Parallelism and Superscalar Processor. Control Unit Operation. Microprogrammed Control. Parallel Processing. Multicore Computers. Number Systems. Digital Logic. The IA64 Architecture. Originally Shared for.

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Mashhoods Web FamilyComputer organization refers to the operationalExamples of architectural attributes include the instruction set, the number of bitsOrganizational attributes include thoseComputer structure refers to the way in which the components of a computer areData processing; data storage; data movement; and control. Central processing unit CPU Controls the operation of the computer andMain memory Stores data. System interconnection Some mechanism that provides for communicationControl unit Controls the operation of the CPU and hence the computer. Arithmetic and logic unit ALU Performs the computers data processingRegisters Provides storage internal to the CPU. CPU interconnection Some mechanism that provides for communication amongThe computer gets its instructions by readingA main memory, which stores both data and instructions an arithmetic and logicGates, memory cells, and interconnections among gates and memory cells. Moore observed that the number of transistors that could be put ona single chipSimilar or identical instruction set In many cases, the same set of machineThus, a program thatSimilar or identicalIncreasing memory size In going fromIncreasing cost In going from lower to higherIna microprocessor, all of the components of the CPU are on asingle chip.Opcode OperandDuring the executeMemory places the contents of the memory locationThis data is then transferred to the MBR. To write a valueThe CPU also places the data it wants to write into the MBR. The CPU then assertsMemory transfers the data on the data bus into theWhen an address is presented to amemoryIn particular, memory systems and. A system is only as fast asA more accurate measure is to runThe systems can be compared to each other on how longAccording to Apple

Computer, the G4 isIf we could have an arbitrary number ofFor integers,CPU time to execute the same set of benchmark programs.ForProgram 2 0.1 1 5. Program 3 0.2 0.1 2. Program 4 1 0.125 1.

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Arithmetic Rank Harmonic RankComputer A 25.325 1 0.25. Computer B 2.8 3 0.21. Computer C 3.26 2 2.1 1BenchmarkProcessor. BenchmarkBased on a R is theBased on b, M is the slowestBenchmarkBenchmarkUsing the geometric mean, R is the slowest no matter which machine is usedBenchmarkGeometric 1 1 1Normalized to Y. Processor. BenchmarkGeometric 1 1 1Machine Y is twice as fast as machine X for benchmark 1, but half as fast forWhen the geometric mean is used, the three machines are shown to have equalAssuming the same instruction mix means that the additional instructions forArithmetic and logic 1 60%. Branch 4 12%. Memory reference with cache 12 10%Using Equation 2.2, we. For the singleprocessorThe answer to this question depends on how we interpret Amdahls law. ThereFirst, there are additionalSecond, there is contentionBut based on the informationThus the actual speedup is only aboutInstruction address calculation iac Determine the address of the next instructionOperand store os WriteThis 1 reduces propagationSystem pins Include the clock and reset pins. Address and data pins Include 32Interface control pins. Control the timing of transactions and provide coordination among initiators andError Reporting pins Used to report parity andCache support pins These pins are needed to support aScan Pins These signal lines support testingStep 5 7006 IR; Step 6 AC — Device 6This value is loadedSeporpoChe value in location 301 which is the instruction with the value 5941 isThe address portion of the IR 941 is loaded into the MAR. BR, and the PC is incremented. These twoThe address portion of the IR 941 is loaded into the MAR.

However, because the data bus is only 16 bits, itFor a 32bit address, one may assume the first half willTypically, a 32bit microprocessorIf the instruction register is to contain the whole instruction, it will have to beIn cases a and b, the microprocessor will be able to access 216 — 64K bytes; theFor case c,Doubling the frequency may mean adopting a new chip manufacturing technologyIn the first case, theThe INPR will only accept data fromWhen the CPU has data to send to the Teletype, it checks FGO. OUTER and sets FGO to 0. The Teletype sets FGI to 1 after the word is printed.The CPU, which is much fasterIf interrupts are used,The 16bit microprocessor has twiceThis requires that theThe lowestpriority device is assigned priority 16. This device must defer to all theAt the beginning of any slot, if none of the TR lines is asserted, only the priority 16Thus, memory must place the data onThe clock period is 125 ns. Therefore, two clock cycles need to be inserted. From Figure 3.19, the Read signal begins to rise early in T. To insert two clockTherefore, the WriteA bus cycle takes 0.25 us, soa memory cycle takes 1 us. If both operands are evenIf one is oddaligned, the timeOn average, they consist of 20 32The number of bus cycles required for the. For the 32bit microprocessor, theHe ODED PSWait State Wait State Wait StateDirect access Individual blocks orAccess is accomplishedRandom access Each addressable location inThe time toItis possible to organize data across a memory hierarchy such that the percentageIna cache system, direct mapping maps each block of main memory into only oneIn setassociative mapping, the cache is dividedOne field identifies a unique word or byte within a block of main memory. TheThese two fieldsA tag field uniquely identifies a block of main memory. A word field identifies aOne field identifies a unique word or byte within a block of main memory.

TheThese two fieldsSpatial locality refers to the tendency of execution to involve a number of memoryTemporal locality refers to the tendency foraTherefore, 4 bits are needed toTherefore, theTherefore, 7 bits are needed to specify the word.Therefore 8 bits are needed to identify the setMain memoryAssociativity 4QaEach line consists ofBytes with addresses 0001 1010 0001 1000 through 0001 1010 0001 1111 areBecause two items with two different memory addresses can be stored in theThe tag is used to distinguish between them.Solution Manual Computer Organization And Architecture 8th Edition.pdf 6 reviews. Instant download and all chapters are included.

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